SEMICONDUCTOR

D040N06G

90A 60V N-Channel Enhancement Mode Power MOSFET

Features

- Fast switching
- Extremely low on-resistance RDS(on)
- 100% single pulse avalanche energy test

Product Summary			
V_{DS}	$R_{DS(on)}$ (mΩ) Typ	I_D (A)	Qg (Typ)
60V	4.0 @ 10V 30A	90	30nc

Mechanical Data

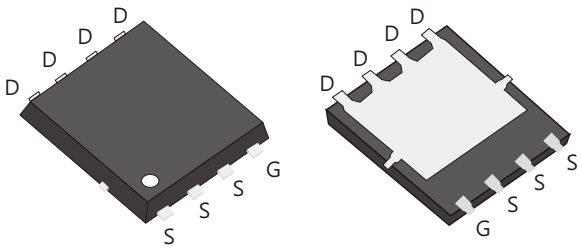
- Case:DFN5×6 Package

DFN5×6

D040N06G

Application

- Switching Application
- SR (Synchronous rectification)
- DC/DC converter
- General purpose applications



Ordering Information

Part No.	Package Type	Package	Quality(box)
D040N06G	DFN5×6	Tape & Reel	5000

Block Diagram

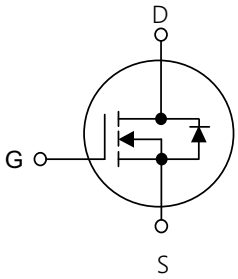


Table1 Absolute Maximum Ratings (T_C=25°C, unless otherwise specified)

Parameter		Symbol	Value	Unit
Drain-Source Voltage		V_{DS}	60	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current (Note 5)	T_C=25°C	I_D	90	A
	T_C=100°C		55	
Pulsed Drain Current (Note 1)		I_{DM}	360	A
Single Pulse Avalanche Energy(Note 2)		E_{AS}	272	mJ
Power Dissipation	T_C=25°C	P_D	78	W
Operating Junction and Storage Temperature		T_J/T_{STG}	-55~+150	°C

Table 2.Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal resistance Junction to Ambient,,Max	$R_{\theta JA}$	50	°C/W
Thermal resistance Junction to Case,Max	$R_{\theta JC}$	1.6	°C/W

Table 3. Electrical Characteristics (T_J=25°C, unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Off Characteristics							
Drain-Source Breakdown Voltage		BV_{DSS}	V_{GS}=0V,I_D=250μA	60	-	-	V
Drain-Source Leakage Current		I_{DSS}	V_{DS}=60V,V_{GS}=0V	-	-	1	μA
Gate- Source Leakage Current	Forward	I_{GSS}	V_{GS}=20V,V_{DS}=0V	-	-	100	nA
	Reverse		V_{GS}=-20V,V_{DS}=0V	-	-	-100	nA
On Characteristics(Note 3)							
Gate Threshold Voltage		$V_{GS(TH)}$	V_{DS}=V_{GS},I_D=250μA	1.0	1.6	2.5	V
Static Drain-Source On-State Resistance		$R_{DS(ON)}$	V_{GS}=10V,I_D=30A	-	4.0	4.8	mΩ
Dynamic Characteristics(Note 4)							
Input Capacitance		C_{ISS}	V_{DS}=30V,V_{GS}=0V,f=1MHz	-	2139	-	pF
Output Capacitance		C_{OSS}		-	708	-	pF
Reverse Transfer Capacitance		C_{RSS}		-	39	-	pF
Switching Characteristics (Note 4)							
Turn-On Delay Time		td(on)	V_{DS}=30V,R_{GEN}=5Ω V_{GS}=10V,I_D=20A,	-	6.5	-	ns
Turn-On Rise Time		t_R		-	8	-	ns
Turn-Off Delay Time		td(off)		-	38	-	ns
Turn-Off Fall Time		tf		-	16	-	ns
Total Gate Charge		Q_G	V_{DS}=30V,I_D=20A, V_{GS}=10V	-	30	-	nC
Gate-Source Charge		Q_{GS}		-	4.3	-	nC
Gate-Drain Charge		Q_{GD}		-	6	-	nC
Drain-Source Diode Characteristics and Maximum Ratings							
Drain-Source Diode Forward Voltage		V_{SD}	V_{GS}=0V, I_S=30A	-	-	1.2	V
Maximum Continuous Drain-Source Diode Forward Current		I_S		-	-	90	A

Notes：1 Repetitive Rating:Pulse width limited by maximum junction temperature
2 L=0.3mH,Starting T_J=25°C
3 Pulse Test: Pulse width ≤300μS, Duty cycle≤2%
4 Guaranteed by design,not subject to production

Typical Characteristics Diagrams

Figure 1.Output Characteristics

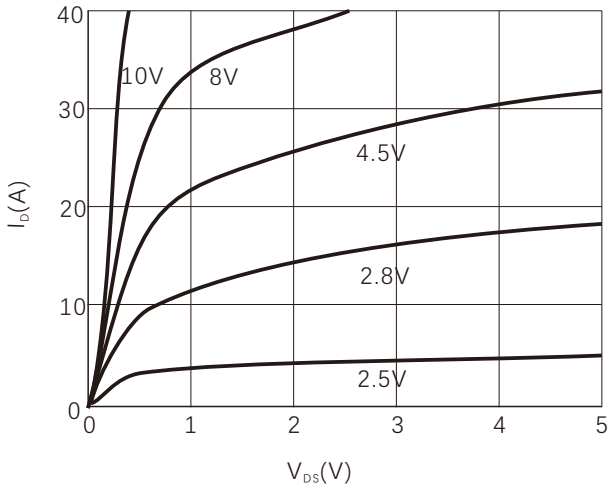


Figure2.Normalized $R_{DS(ON)}$ vs Temperature

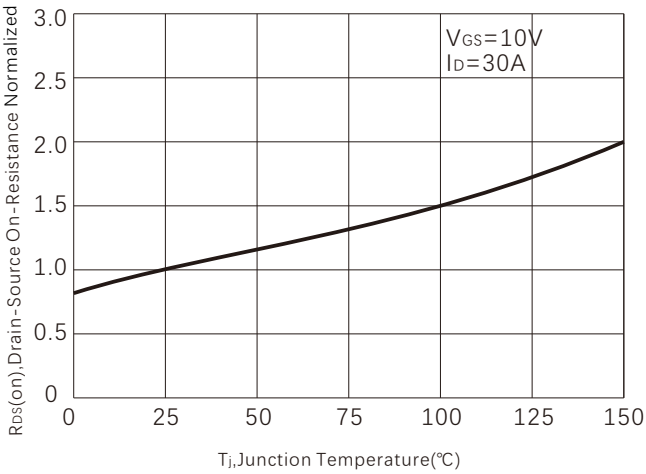


Figure 3.On-Resistance vs.Drain Current

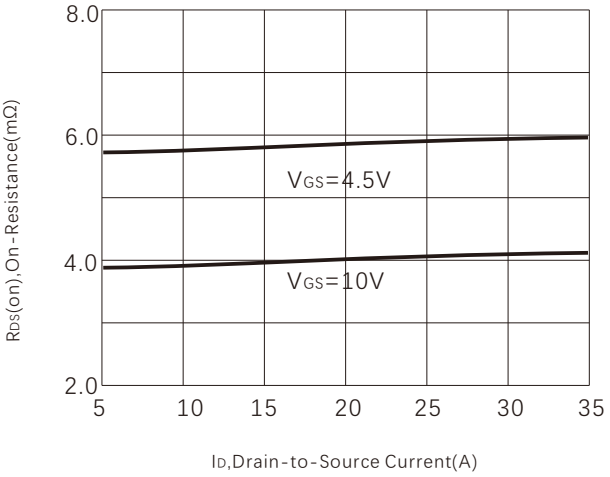


Figure 4. Capacitance

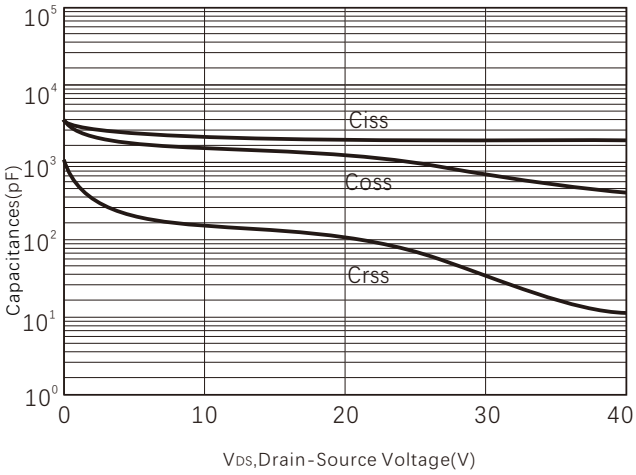


Figure 5.Gate charge

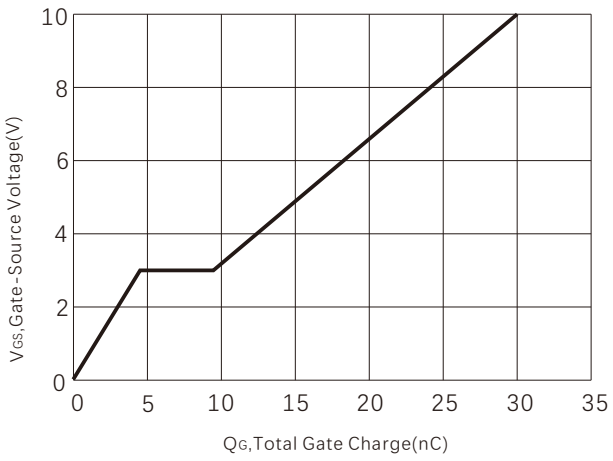


Figure 6.Source-Drain Diode Forward Voltage

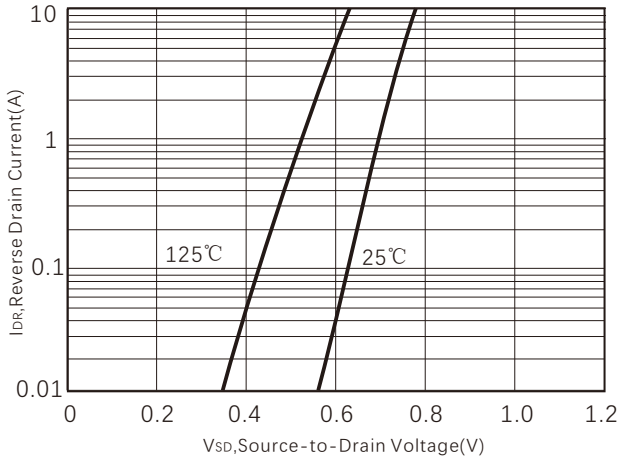


Figure7.Maximum Drain Current vs Temperature

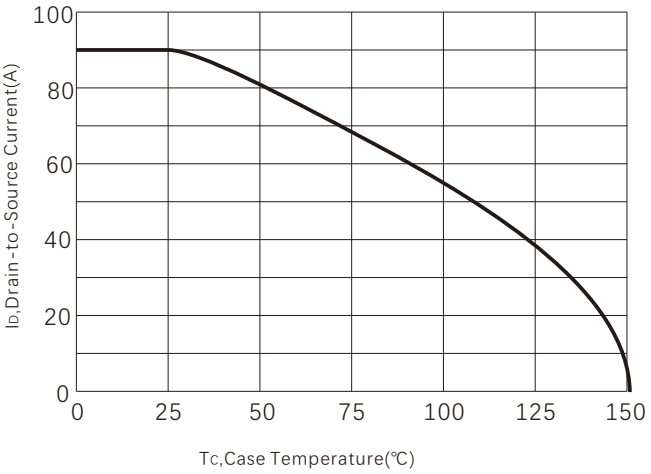


Figure 8. Power dissipation

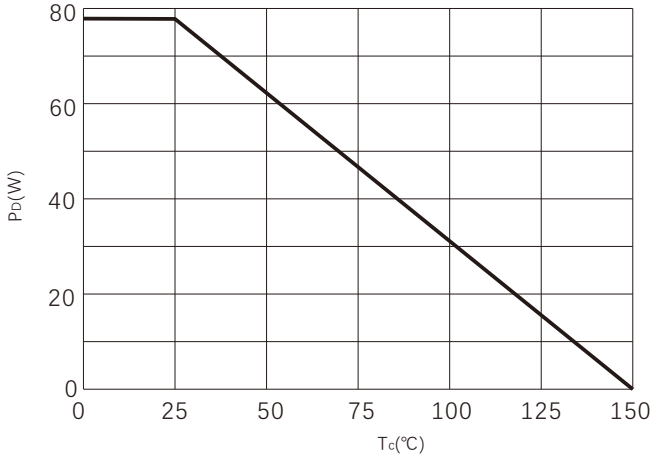


Figure 9.

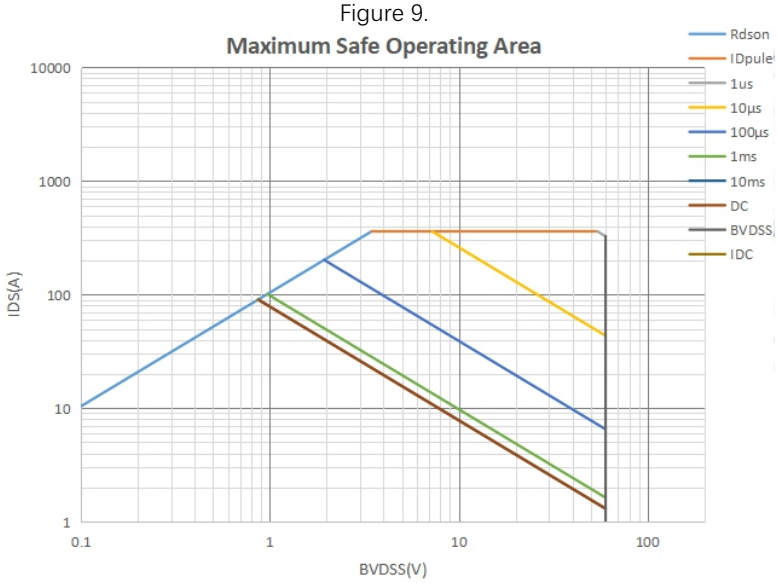
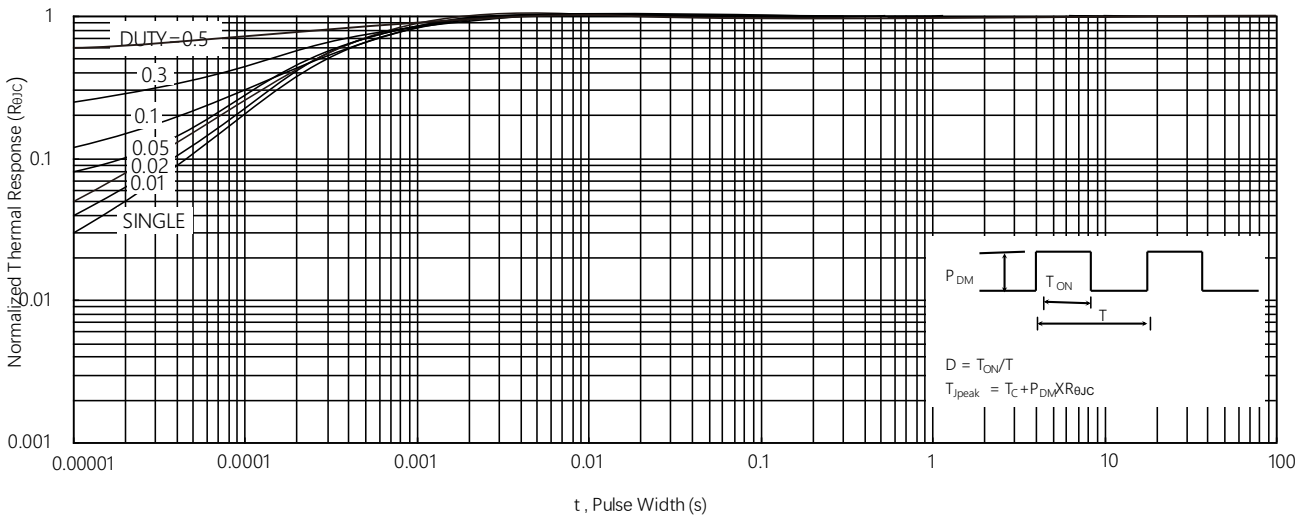
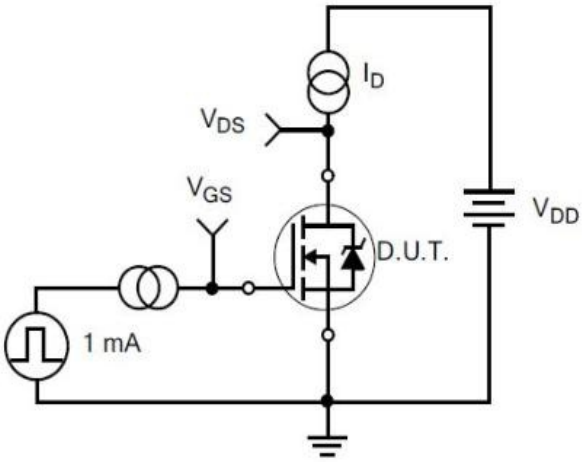


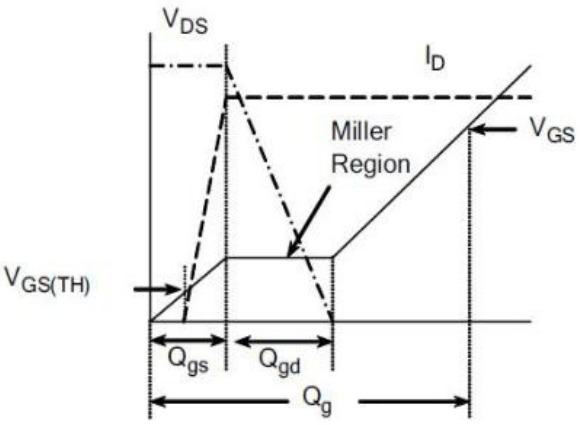
Figure 10.Normalized Maximum Transient Thermal Impedance



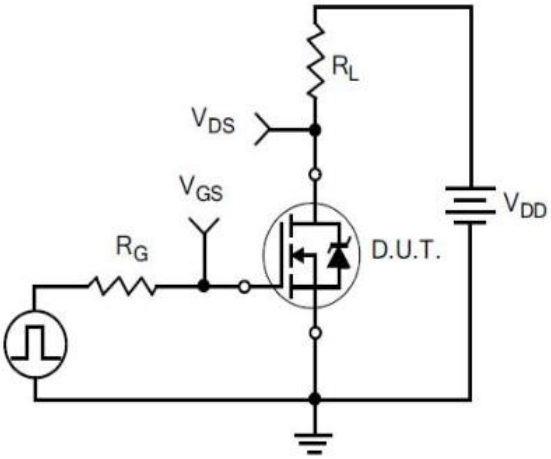
Typical Test Circuit



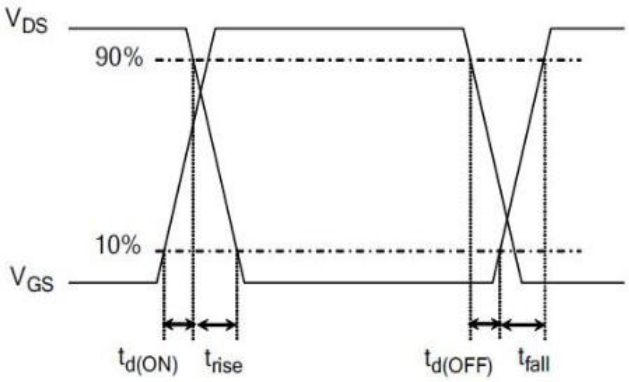
1) Gate Charge Test Circuit



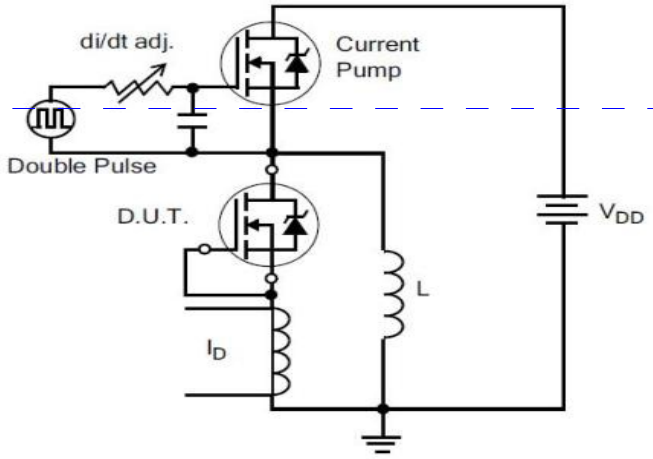
2) . Gate Charge Waveform



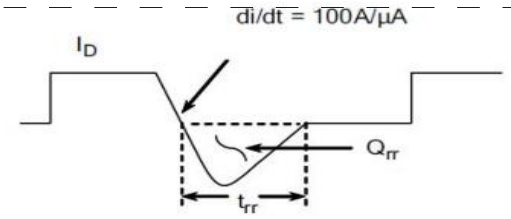
3) Resistive Switching Test Circuit



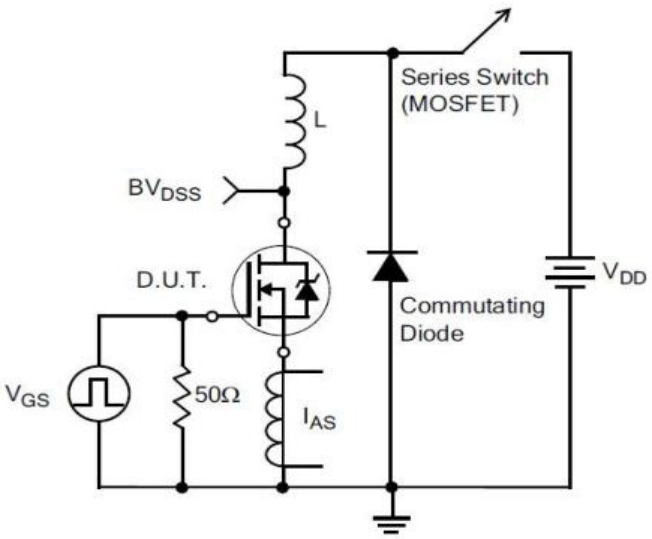
4) Resistive Switching Waveforms



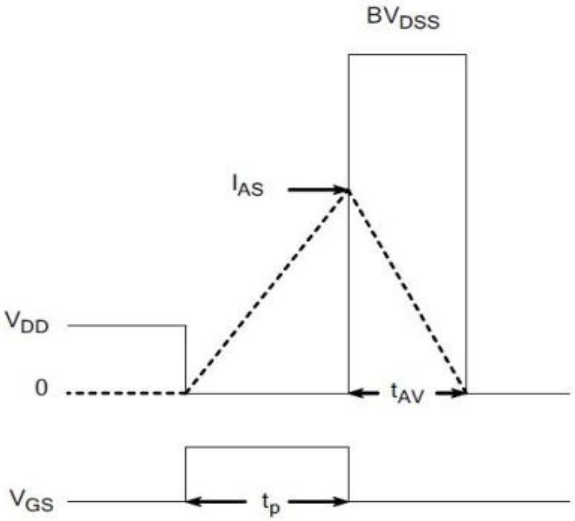
5) Diode Reverse Recovery Test Circuit



6) Diode Reverse Recovery Waveform



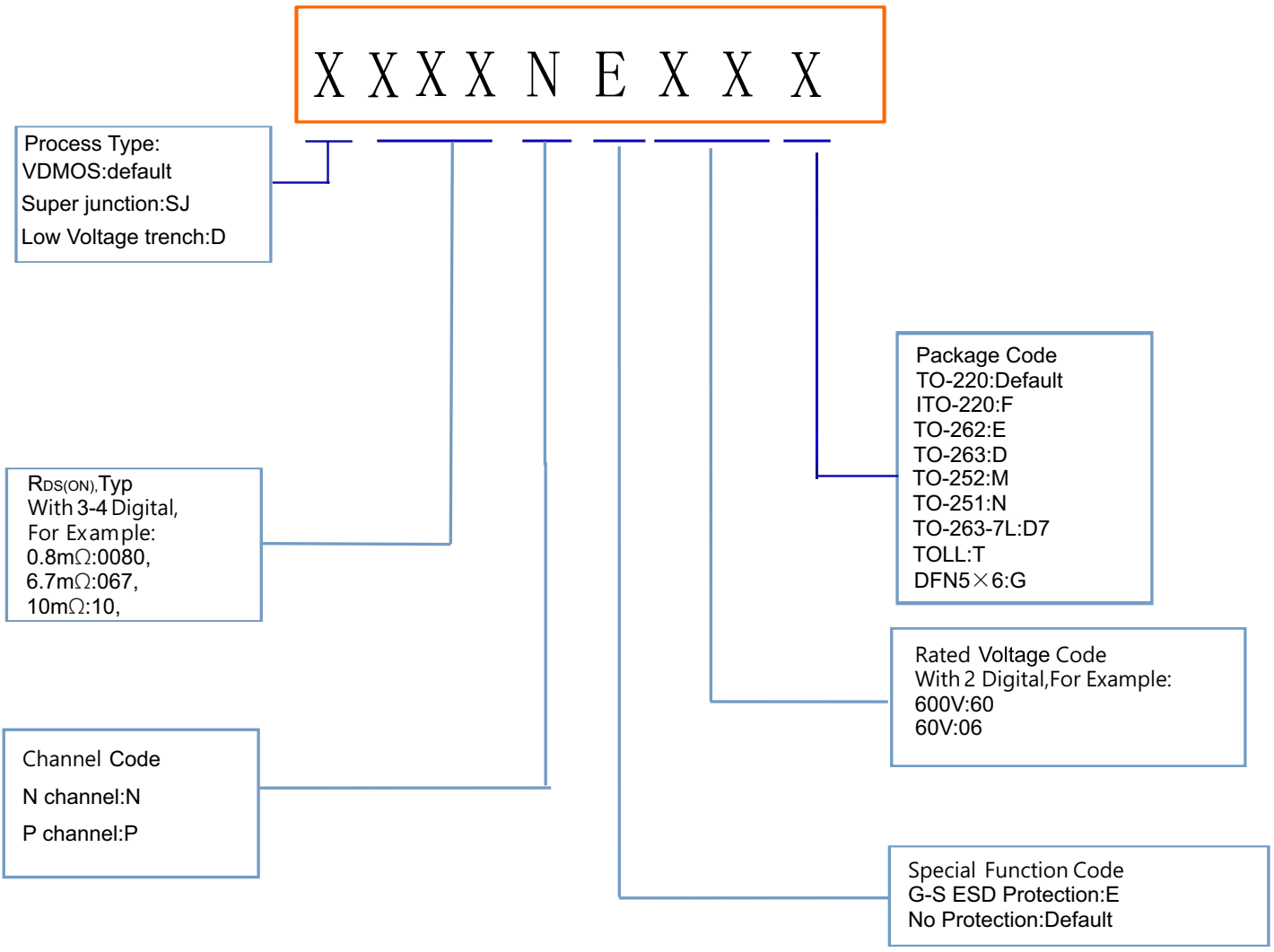
7) . Unclamped Inductive Switching Test Circuit



$$E_{AS} = \frac{I_{AS}^2 L}{2}$$

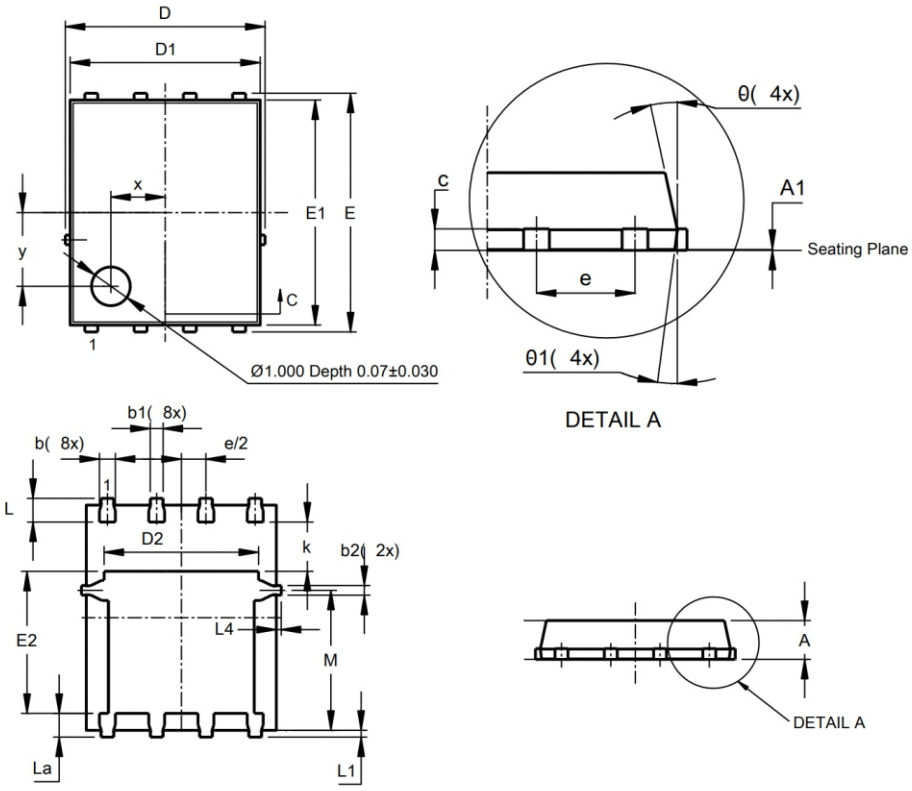
8) Unclamped Inductive Switching Waveforms

Product Names Rules



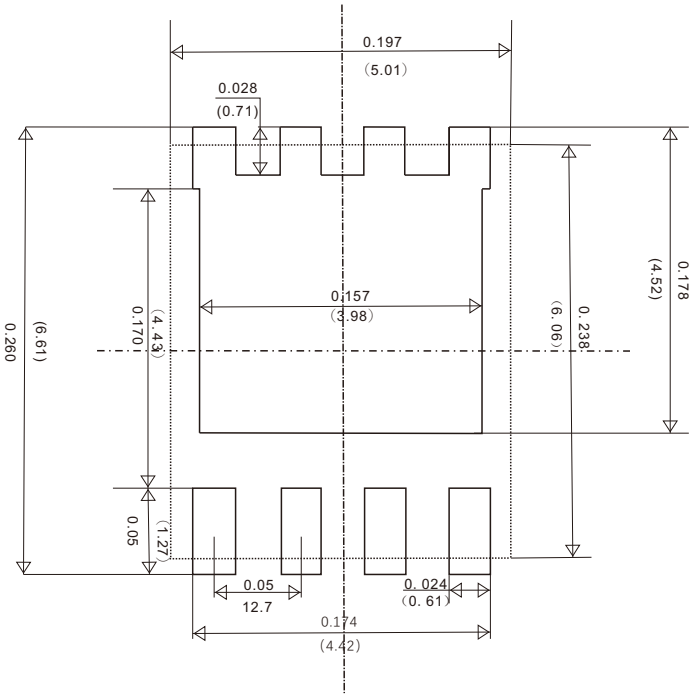
Dimensions

DFN5×6 PACKAGE OUTLINE DIMENSIONS



Dim	Min	Max	Type
A	0.90	1.10	1.00
b	0.23	0.41	0.32
b1	0.24	0.30	0.27
b2	0.16	0.32	0.23
c	0.17	0.27	0.22
D	-	-	5.01
D1	4.80	4.95	4.88
D2	-	-	3.98
E	-	-	6.06
E1	5.72	5.82	5.77
E2	3.42	3.52	3.47
k	-	-	1.33
L	0.56	0.66	0.61
La	0.57	0.67	0.63
L1	0.06	0.15	0.11
L4	-	-	0.06
M	3.00	3.20	3.08
Φ	10	11	10.39

Suggested Pad Layout



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